

Terry N. Holdt
420 Barker Drive
West Chester, Pennsylvania 19380
Phone: 215-692-7314

PERSONAL:

Date of Birth: August 8, 1943
Height/Weight: 6'1", 205 pounds
Married, three children

EDUCATION:

BSEE, University of Illinois, 1967; with honors
MSEE, University of Illinois, 1968; with honors
Member of Tau Beta Pi, Eta Kappa Nu

PROFESSIONAL EXPERIENCE:

August 1974 to present- Product/Program Manager for
Microcomputers

In this function, I report to the company president and have responsibility for the overall program planning and execution of efforts surrounding the microprocessor system. This includes participation in decisions regarding product definition, pricing, support activities (hardware and software), customer interface, advertising, factory planning, allocation of available resources and process development. The latter responsibility was one I agreed to perform on an interim basis since management of the process development group was lacking. This evolved into a nearly full time job with responsibility for the labor force, supervision and a portion of the engineering of the N channel Silicon Gate Depletion Load 5 Volt Process. My own responsibilities during this period involved definition of experiments and analysis of results requiring knowledge of implant dose and energy designs and detailed analysis of critical electrical parameters including mobilities, body effect, gains and critical circuit capacitances. Thus while my primary function was to manage the overall microprocessor program, my primary effort was management and technical assistance in the process development area.

March 1974 to August 1974- Product Manager-MOS P/N
Logic Products
(Motorola Semiconductor
Products, Division)

Primary responsibility in this role was P&L control over the M6800 family of microprocessors. This included responsibility for Product Engineering, Test Engineering and Test Direct Labor for MOS Logic products as well as P&L responsibility (down to gross margin) for the line. The effort expended on the microprocessor and associated products (PIA and ACIA) was early in their stage of introduction and much effort was expended by my groups in debugging and characterizing the products.

July 1973 to March 1974- Product Manager-MOS P/N Metal Gate Products
(Motorola)

Responsibility included Product Engineering, Test Engineering, Test Direct Labor, Process Engineering (Sustaining and Development), and Process Direct Labor. Basically, I had control of the entire line necessary to build the product with the sole exception of assembly, the bulk of which was done offshore and which was used by all product groups such as mine on an allocated basis.

Responsibilities of groups under my control included yield enhancement, overall cost minimization, customer interface, test program development, and analysis of available testers on the market to do the job. Forecasting of P&L goals was a prime task which involved both short term (by line item down to Gross Margin) and long term (every line item down to Profit Before Taxes) factory cost analysis.

Products included Logic (Custom and Standard), RAM's and ROM's. My line had a run rate of approximately \$10.5 million/year and I was responsible for approximately 25 engineers, 20 technicians, 5 foreman and 170 direct labor operators. Process technology was MOS Metal Gate, P channel and N channel with three shifts of operation.

December 1972 to July 1973- Product Manager-MOS P/N Metal Gate Products
(Motorola)

Responsibilities in this period were identical to those from July 1973 to March 1974 with exception of not having the wafer area under my control.

March 1971 to December 1972- Manager, P/N MOS Product Engineering
(Motorola)

Supervisory responsibility for seven engineers and four technicians. Tasks included establishment and maintenance of a functioning liason between the Product Engineer and the groups with which they must interface: Wafer Processing, Assembly, Test, Design and Q.C. Also included in the job was active participation in decisions involving business opportunities to be pursued by the product group.

December 1969 to March 1971 - Section Manager, P/N MOS Product Engineering
(Motorola)

Responsibility for four engineers and three technicians in the Product Engineering Group.

July 1969 to December 1969- Product Engineer, P/N MOS
Product Engineering
(Motorola)

July 1968 to July 1969- Engineering Trainee
(Motorola)

This year was spent on the Motorola Engineering Training Program which consisted of three month rotations in the following four areas:

- 1.) DTL Wafer Processing
- 2.) Device Design-Bipolar
- 3.) Circuit Design-Bipolar
- 4.) Product Engineering-MOS

EDUCATION:

PROFESSIONAL EXPERIENCE:

August 1974 to present Product/Program Manager for Microcomputers

In this function, I report to the company president and have responsibility for the overall program planning and execution of efforts surrounding the microprocessor system. This includes participation in decisions regarding product definition, pricing, support activities (hardware and software), customer interface, advertising, factory planning, allocation of available resources and reports to management. The latter responsibility was one I agreed to perform on an interim basis since management of the process development group was lacking. This involved both a nearly full time job with responsibility for the labor force, supervision and a portion of the engineering of the 4 channel Silicon Gate Isolation Lead 1. Work Process. My responsibilities during this period included definition of experiments and analysis of results requiring knowledge of critical process and energy designs and detailed analysis of critical electrical parameters including reliability, delay effect, jitter and critical circuit capacitance. While my primary function was to manage the overall microprocessor system, my primary effort was management and technical assistance in the process development area.

March 1974 to August 1974 Product Manager-MOS P/N Logic Products
(Motorola Semiconductor Products Division)

Primary responsibility in this role was full control over the MOSIC family of microprocessors. This included responsibility for Product Engineering, Test Engineering and Test Circuit Layout for MOS Logic Products as well as full responsibility (down to gross margin) for the line. The effort expended on the microprocessors and associated products (PLA and MLI) was early in their state of development and such effort was expended to establish manufacturing and characterizing the products.