United States Patent [19]

Paivinen et al.

[11] **4,011,105**

[45] **Mar. 8, 1977**

[54] **FIELD INVERSION CONTROL FOR N-CHANNEL DEVICE INTEGRATED CIRCUITS**

[75] Inventors: **John O. Paivinen**, Newtown Square; **Walter D. Eisenhower**, Audubon, both of Pa.

[73] Assignee: **MOS Technology, Inc.**, Norristown, Pa.

[22] Filed: **Sept. 15, 1975**

[21] Appl. No.: **613,537**

[52] **U.S. Cl.** **148/1.5**; 148/187

[51] **Int. Cl.**[2] **H01L 21/265**

[58] **Field of Search** 148/1.5, 187

[56] **References Cited**

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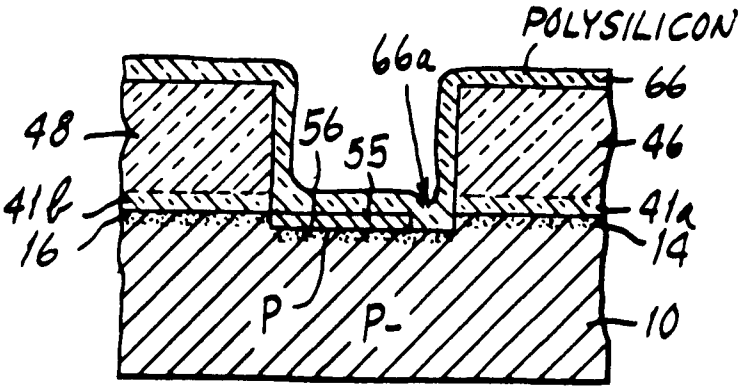
Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—J. M. Davis
Attorney, Agent, or Firm—Cooper, Dunham, Clark, Griffin & Moran

[57] **ABSTRACT**

The field inversion properties of integrated circuits incorporating N-channel MOS devices are improved by using a silicon substrate whose bulk dopant concentration is low, but whose local dopant concentration is high at the field surfaces under the field oxide separating the active surface areas where the individual N-channel MOS devices are formed. The differential doping between surface areas under the field oxide and the active surface areas of the substrate is done by nonselectively ion-implanting boron into the substrate to form a uniform low resistivity layer, removing selected portions of the low resistivity layer to expose the unimplanted, high resistivity substrate and forming the active devices at the unimplanted substrate portions. As an option, the unimplanted surface portion can be doped to an intermediate dopant concentration to improve performance. The remaining pattern of the low resistivity layer is covered with field oxide. The invention allows the use of relatively inexpensive, low dopant concentration substrates to conveniently manufacture high performance N-channel MOS integrated circuits.

10 Claims, 16 Drawing Figures



United States Patent [19]

Paivinen et al.

[11] **4,074,301**

[45] **Feb. 14, 1978**

[54] **FIELD INVERSION CONTROL FOR N-CHANNEL DEVICE INTEGRATED CIRCUITS**

[75] Inventors: **John O. Paivinen**, Newtown Square; **Walter D. Eisenhower**, Audubon, both of Pa.

[73] Assignee: **MOS Technology, Inc.**, Norristown, Pa.

[21] Appl. No.: **737,547**

[22] Filed: **Nov. 1, 1976**

Related U.S. Application Data

[62] Division of Ser. No. 613,537, Sept. 15, 1975, Pat. No. 4,011,105

[51] **Int. Cl.**[2] **H01L 29/78**

[52] **U.S. Cl.** **357/23**; 357/91; 148/1.5; 148/187

[58] **Field of Search** 357/23, 91; 148/1.5, 148/187

[56] **References Cited**

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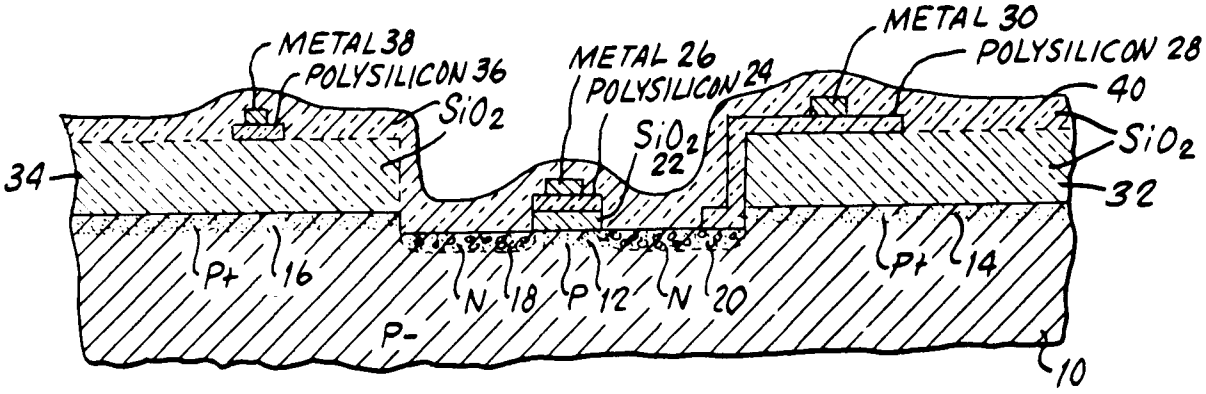
Primary Examiner—Andrew J. James
Attorney, Agent, or Firm—Cooper, Dunham, Clark, Griffin & Moran

[57] **ABSTRACT**

The field inversion properties of integrated circuits incorporating N-channel MOS devices are improved by using a silicon substrate whose bulk dopant concentration is low, but whose local dopant concentration is high at the field surfaces under the field oxide separating the active surface areas where the individual N-channel MOS devices are formed. The differential doping between surface areas under the field oxide and the active surface areas of the substrate is done by nonselectively ion-implanting boron into the substrate to form a uniform low resistivity layer, removing selected portions of the low resistivity layer to expose the unimplanted, high resistivity substrate and forming the active devices at the unimplanted substrate portions. As an option, the unimplanted surface portion can be doped to an intermediate dopant concentration to improve performance. The remaining pattern of the low resistivity layer is covered with field oxide. The invention allows the use of relatively inexpensive, low dopant concentration substrates to conveniently manufacture high performance N-channel MOS integrated circuits.

8 Claims, 16 Drawing Figures



United States Patent [19]

Paivinen et al.

[11] **4,212,100**

[45] **Jul. 15, 1980**

[54] **STABLE N-CHANNEL MOS STRUCTURE**

[75] Inventors: **John Paivinen**, Bloomfield Hills, Mich.; **Walter D. Eisenhower, Jr.**, Audobon, Pa; **Ernest R. Helfrich**, Richardson, Tex.

[73] Assignee: **MOS Technology, Inc.**, Norristown, Pa.

[21] Appl. No.: **835,985**

[22] Filed: **Sep. 23, 1977**

[51] **Int. Cl.**[3] **B01J 17/00**

[52] **U.S. Cl.** **29/571**; 29/578; 357/23; 357/59

[58] **Field of Search** 29/571, 578; 357/59

[56] **References Cited**

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Primary Examiner—W. C. Tupman

Attorney, Agent, or Firm—Cooper, Dunham, Clark, Griffin & Moran

[57] **ABSTRACT**

An N-channel MOS integrated circuit device having a composite metal gate structure which has improved temperature stability. The gate structure uses a polysilicon layer to separate the conventional metal gate from the conventional underlying gate oxide. The metal gate and the polysilicon layer extend laterally at least to the lateral extent of the gate region. This composite metal gate structure improves the temperature stability of the IC, and may be used, for example, in read-only memory (ROM) applications. The polysilicon layer is formed without additional photolithographic steps.

2 Claims, 15 Drawing Figures