EFFECT OF GATE OXIDE THICKNESS VARIATIONS
ON IMPLANTED ENHANCEMENT AND DEPLETION DEVICES

In the classical enhancement device fabricated on a uniform substrate, the threshold voltage increases as the gate oxide thickness increases. The same is true for any implanted enhancement device where the implant is sufficiently deep that the amount of charge entering the silicon is not affected by variations in gate oxide thickness. However, as pointed out in "Threshold Voltage Stabilization in N-Channel Implanted Enhancement Devices," a shallower implant can be found where variations in gate oxide thickness change the amount of charge which is implanted in the silicon so as to achieve a constant threshold voltage. As a further extrapolation of this technique, an even shallower implant will permit an absolute reversal of behavior: that is, the threshold voltage will decrease as the gate oxide thickness increases. This last approach has the interesting potential that the decrease in k' caused by an increase in gate oxide thickness could be offset by a decrease in threshold voltage (at least for circuits operating with low values of V_D): thus, with suitable selections in process, an enhancement mode device appears achievable with a stabilized current characteristic.

Unfortunately, all of these actions have a deleterious effect on a depletion mode device subsequently fabricated onto the same wafer as an implanted enhancement device. First, with no changes in doping concentration, an increase in gate oxide thickness makes it more difficult to pinch off the depletion mode conduction channel and increases the current required to drive the device. Then, if a thick gate oxide reduces the amount of charge implanted at the enhancement device, the amount of conduction charge at the depletion mode will be increased,

since it is of the opposite polarity to the charge which has been implanted at the depletion mode device in order to form the device in the first place. Consequently, selection of process steps to stabilize the threshold voltage at the enhancement mode device will increase the current at the depletion mode device and the process steps to stabilize the current at the enhancement mode device will even further increase the current at the depletion mode device. This tendency, of course, will be lessened if the depletion implant decreases with increases in gate oxide thickness: however, we are deliberately using a deeper depletion implant than enhancement implant in order to achieve a fast pinch-off for the depletion device so that this countereffect is weaker than might otherwise be achieved.

These consequences are summarized qualitatively in Figure 1 which shows the characteristic for an enhancement device and a depletion device in an inverter stage with the enhancement device fully conductive. The change from normal gate oxide to thick gate oxide is assumed to have occurred without accompanying changes in implanted charge, a condition that really does not occur in practice; however, such change would be accompanied by an increase in threshold voltage from V_{T_1} to V_{T_2}. Our current process development is accompanied by sufficient reduction in implanted charge so that condition (3) is almost precisely achieved with the consequent stabilization of the threshold voltage at V_{T_1}. It should be noted that the change from (1) to (3) for the inverter stage, with an unchanging threshold voltage, represents an added noise voltage in the system as compared to standard process where enhancement mode devices are used as load resistors: <u>the added noise voltage must be considered in the circuit design</u>. Stabilization of the enhancement device current, resulting in a change from (3) to (4) further increases the ON-current and reduces the threshold voltage from V_{T_1} to V_{T_3} so that an increase in power consumption is

accompanied by further jeopardy in noise voltage, thereby representing a loser on two counts.

The most desirable approach is obviously the control of the gate oxide thickness so that any variation is vanishingly small. However, to the extent that this is not reasonably achievable in the process, an adverse effect in circuit operation arises which must be considered in the design approach.

TEAM 6502 .ORG

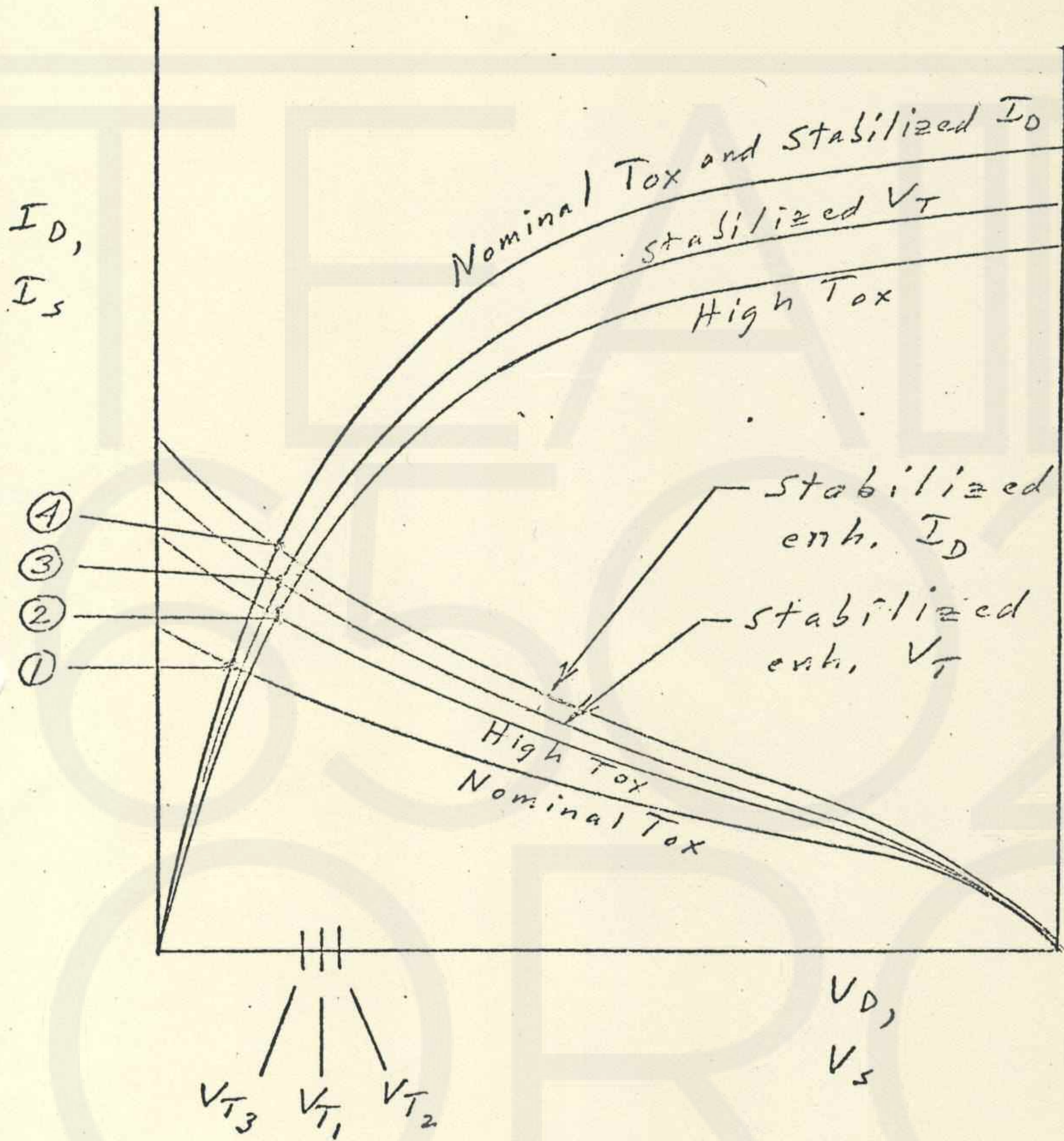

Figure 1