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DESIGN OF A P-JFET FOR THRESHOLD VOLTAGE TRANSLATION AND DEPLETION MODE OPERATION

Using the guideline of "Implant for a 'Constant' Concentration Near the Surface," one can choose an implant profile approximating that shown in Figure 1; that is, one can achieve some approximation of a "constant" concentration. The remaining task is to pick a charge value for the implant which will provide the desired electrical operation. The two objectives usually sought are (1) threshold voltage translation and (2) depletion mode operation.

Threshold Voltage Translation

When a boron implant is used to reduce the threshold voltage of a P-channel MOS, the resulting profile corresponds to Figure 1. As with a depletion mode device, two depletion regions are formed in the implant, a surface depletion layer (as is expected with any P-surface) and a backside depletion layer which forms with any metallurgical junction. The total charge must be low enough that these two depletion layers will totally deplete the implanted charge with the gate at zero volts: otherwise, a conductive leakage path is formed. Further, the charge must also be low enough so that the two depletion layers will not separate to form a conductive channel (the appearance of which signifies the "threshold voltage" for the device) until the gate is at some desired voltage required for proper circuit operation. To assist in this design process, use is made of the four sets of curves attached hereto.

If one follows the design approach of the above-referenced memo, the heat treatment subsequent to the implant dominates the design calculations. Since we are working with a boron implant, the above memo establishes that:

$$\overline{R}_p = x_0 + 0.01 + \sqrt{\pi Dt + 0.019\, x_0}$$

Thus the center of the implant is fixed by the subsequent heat treatment. In the same memo it is established that the "constant" concentration is equal to

$$(C_{peak})_1 = \frac{0.282\, Q}{\sqrt{\frac{\sigma_0^2}{2} + Dt}}$$

Although this is a half-plane normal distribution, we can establish an effective depth for the latter as shown in Figure 2 by defining that

$$X_{eff} = \frac{Q/2}{(C_{peak})_1}$$

$$= \frac{\frac{1}{2}\sqrt{\frac{\sigma_0^2}{2} + Dt}}{0.282}$$

$$= \frac{\sqrt{\frac{\sigma_0^2}{2} + Dt}}{0.564}$$

Therefore, we have established the total depth X_i of the implant as being

$$X_i = 0.01 + \sqrt{\pi Dt + 0.019\, x_0} + \frac{\sqrt{\frac{\sigma_0^2}{2} + Dt}}{0.564}$$

Thus we have approximated the actual implant by a constant concentration profile as shown in Figure 3.

If our P-channel manufacturing process results in

$$\frac{Q_{ss}}{C_0} = 0.9^{v}$$

then the flat-band voltage on a N-channel device would be 1.8 volts. If we wish to have an effective threshold voltage of 0.8 volts when viewed as a P-channel device, we must find a concentration value for the implant such that the thickness

of the surface depletion layer added to the thickness of the back depletion layer is exactly equal to X_i from above. Referring to Figure 4, this means that for

$$|V_G - V_{FB}| = 1.0^V$$

and for $Dt = 0.002\ \mu^2, x_0 = 0.105\ \mu$, we can calculate:

$$\bar{R}_p = 0.2054\ \mu \quad \text{(accelerating energy = 64 keV)}$$

$$\sigma_0 = 0.051\ \mu$$

from which

$$X_i = 0.2\ \mu$$

Then, using the charts, "Back Depletion Layer Thickness vs. Implant Concentration" and "Surface Depletion Layer Thickness vs. Implant Concentration," for assumed values of $(C_{peak})_1$, we can look up the following values:

$(C_{peak})_1$	x_s	x_b	$x_s + x_b$
1.5×10^{16}	.113 μ	.058 μ	.171 μ
1.3×10^{16}	.127 μ	.064 μ	.191 μ
1.2×10^{16}	.134 μ	.072 μ	.206 μ

As an approximate solution,

$$(C_{peak})_1 = 1.25 \times 10^{16}$$

Correspondingly, the total charge, N_i, required in excess of substrate concentration is (using charts "Surface Depletion Layer Charge vs. Implant Concentration" and "Back Depletion Layer Charge vs Implant Concentration"):

$$N_i = N_s + N_b$$

$$= 1.65 \times 10^{11} + 0.86 \times 10^{11} = 2.51 \times 10^{11}$$

To this must be added the charge lost in overcoming the substrate concentration which is of opposite polarity. With the half-plane normal distribution, the actual profile at the value of substrate concentration is wider than is implied by the approximation of Figure 3. For instance, with a peak concentration of 1.25×10^{16}, a substrate concentration of 10^{15} results in the half-plane normal distribution's being equal to the substrate concentration at $2.25\ \sigma_1$. For the data cited above, $\sigma_1 = 0.06324\ \mu$. Thus, as shown in Figure 5, the effective width of the implant at 10^{15} is $0.24\ \mu$. This represents a loss of 0.24×10^{11} charge due to the substrate. Therefore the total implant originally made into the silicon has to be

$$N_T = N_i + N_{ss}$$

$$= 2.51 \times 10^{11} + 0.24 \times 10^{11}$$

$$= 2.75 \times 10^{11}$$

Since the center of the implant was at $0.1\ \mu$, while σ_0 was equal to $0.051\ \mu$, only 97.5 percent of the implant reached the silicon. Therefore the implant as measured by the implanter should be 2.82×10^{11}.

Therefore we would specify an implant of 2.82×10^{11} at 64 keV where the subsequent heat treatment is one hour at 950°C. This compares favorably with the empirically determined design used in the 2540 where 2.88×10^{11} with an accelerating voltage of 60 keV are the actual values. (Note that a lesser fraction of the total charge reaches the silicon in the latter circumstance since a lower accelerating voltage is used.)

Depletion Mode Operation

By using the previous design parameters but a much higher total implant charge, one can arrive at a P-JFET that permits operation in the so-called "depletion mode." As shown in Figure 6, the drain is connected to some negative V_{DD} while the gate is tied to the source, the common node moving between V_{DD} and zero volts. This device is used to cause internal voltages to achieve V_{DD} potential in the absence of any more negative supply voltages: this requires that the device be conductive from source to drain even when the gate potential is at V_{DD}. Therefore the total implanted charge must be sufficiently high that an excess of charge is available after the surface depletion layers and the back depletion layer have been accommodated.

If we want depletion mode operation with

$$V_{DD} = 10^V$$

$$V_{FB} = 1.8^V$$

$$X_i = 0.2\ \mu$$

we can arrive at a cut-and-try solution from the attached graphs that $(C_{peak})_1 = 3.5 \times 10^{16}$, a concentration at which the surface depletion layer is 0.09 μ while the back depletion layer is 0.107 μ, for a total depletion layer thickness of .197 μ. Under this circumstance the two depletion layers are almost exactly in contact, with no excess charge available to provide a conductive path to V_{DD}. Since the profile is assumed to be identical to the one above except for peak concentration,

$$N_T = N_i + N_S$$

$$= 7 \times 10^{11} + 0.24 \times 10^{11}$$

$$= 7.24 \times 10^{11}$$

Then, since only 97.5 percent of the implant reached the silicon, the total implant is 7.425×10^{11}. Any useful depletion mode device has to be at an implanted charge in excess of this value.

A closer estimate of the minimum implanted charge that can be used makes use of material covered in "An Equivalent Circuit for the P-JFET in Depletion Mode." The equation given therein for Q_C can be put into the form

$$\frac{Q_C}{.75C_0} = [V_G - V(y)] + \frac{4}{3}\frac{q}{C_0}(N_I - N_{SS}) - \frac{4}{3}\frac{Q_B}{C_0} - .05\frac{q}{C_0}\frac{K_S}{K_0}x_0C_i - V_{FBN}$$

In order that there be a conductive channel when the source is very close to the drain voltage, we must have $Q_C > 0$ for $V_G = V(y) = V_D$. This requires that

$$N_I - N_{SS} > \frac{Q_B|_{V_D}}{q} + .0375\frac{K_S}{K_0}x_0C_i + \frac{3}{4}\frac{C_0}{q}V_{FBN}$$

The predominant manufacturing variables are the substrate concentration and the N-channel flat-band voltage: this relationship must be satisfied under the most adverse conditions for each.

If we assume incoming material with a substrate concentration of $10^{15} \pm 30\%$, $V_D = -9^V$,

$$\frac{Q_B}{q} = 3.52 \times 10^{11} \pm .493 \times 10^{11}$$

Then, if the N-channel flat-band voltage varies from 1.2^V to 1.8^V, we have for $x_0 = 0.105\ \mu$

$$\frac{3}{4}\frac{C_0}{q}V_{FBN} = 2.3148 \times 10^{11} \pm .463 \times 10^{11}$$

Thus,

$$N_I - N_{SS} > 0.0375\frac{K_S}{K_0}x_0C_i + 5.83 \times 10^{11} \pm 0.956 \times 10^{11}$$

Next, if the implant is made at 45 keV, so that 85% of the implanted charge is in the silicon, for which $\sigma_0 = 430\,\text{Å}$, followed by a treatment for

which Dt = 0.0016. Then

$$C_i = (C_{peak})_1 = \frac{0.282\ Q}{\sqrt{\frac{\sigma_0^2}{2} + Dt}}$$

$$= \frac{0.282\left(\frac{N_I}{0.85}\right)}{\sqrt{\frac{.\overline{043}^2}{2} + .0016 \times 10^{-4}}}$$

$$= 6.6 \times 10^4\ N_I$$

Further, if the implant is assumed to be 2500 Å in depth, then $N_{SS} = 0.25 \times 10^{11}$, so that

$$N_I > 0.0375 \times 3 \times 0.105 \times 10^{-4} \times 6.6 \times 10^4\ N_I + 5.83 \times 10^{11} \pm 0.956 \times 10^{11}$$

$$> 0.0779\ N_I + 5.83 \times 10^{11} \pm 0.956 \times 10^{11}$$

Solving,

$$N_I > \frac{5.83 \times 10^{11} \pm 0.956 \times 10^{11}}{0.9221}$$

$$> 6.322 \times 10^{11} \pm 1.04 \times 10^{11}$$

Since N_I has to exceed the largest value that the manufacturing tolerances impose, $N_I > 7.36 \times 10^{11}$, and since only 85% of the implanted charge has reached the silicon, then

$$Q_T = \frac{N_I}{0.85} = 8.66 \times 10^{11}$$

This represents the lowest value of implanted charge for which a device will be conductive to -9^V in the face of the predominant manufacturing tolerances: the current at $V_S = 0$ represents the lowest "ON" current that can be manufactured under the assumptions given. Higher implant charges may be useful and necessary for higher speed circuits, the exact values flowing from computer modeling where

circuit speed is the primary controling variable. It is probably true that one will use depletion modes with larger implant charge for high-speed applications where the better constant-current approximation assists in maintaining the best speed-DC power ratio, whereas one will use low implant charge for those applications where speed is of little consequence and one is seeking to reduce to as low a value as possible the DC power consumption for the circuits.

Finally, one can expect to vary the efficiency of the depletion mode action by changing the depth at which the implant is made. In particular, a shallower implant will permit more effective pinch-off at whatever channel current is desired than will a deep implant. These two extremes are idealized in Figure 7 where the concentration level and implant depth immediately adjacent to the oxide just accommodates the depletion layer formed when the gate and source are held at V_{DD}. Since the higher concentration permits a thinner initial depletion layer, which in turn absorbs a lesser voltage across the resulting capacitance, the structure with a high concentration next to the oxide will be more effective in pinching off a given channel charge than will the structure with a low concentration next to the oxide. Therefore, efficiency is to be found in working with shallow initial implants and letting the heat treatment result in a profile approximating that shown in Figure 8: such profiles are not calculable and are best pursued by experimental methods. This line of thought is supported by the fact that P-JFETs with very satisfactory characteristics have been constructed using accelerating voltages of 45 keV with subsequent heat treatment of one hour at 950°C as compared to the 60 keV used with a 2540 with its subsequent heat treatment of one hour at 950°C and it is possible that the P-JFETs thus far constructed are not yet optimized.

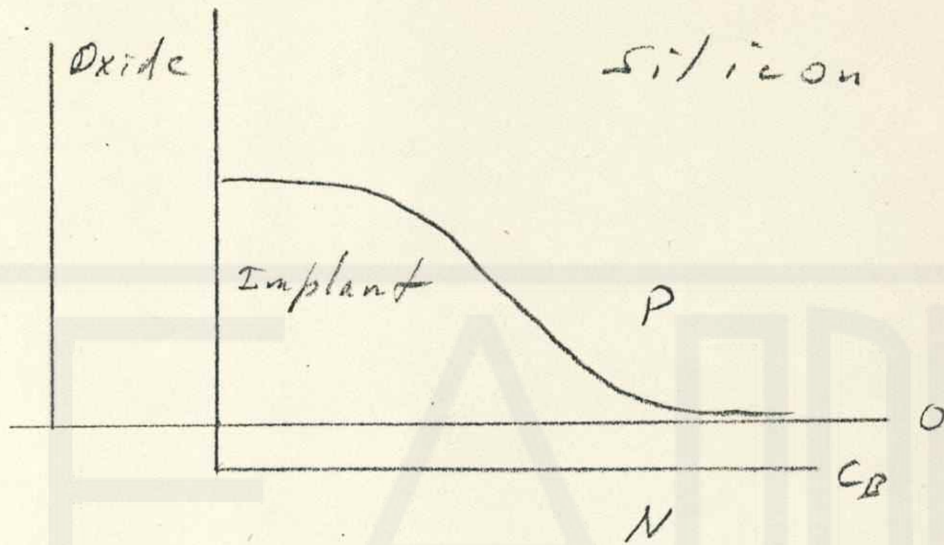

Figure 1

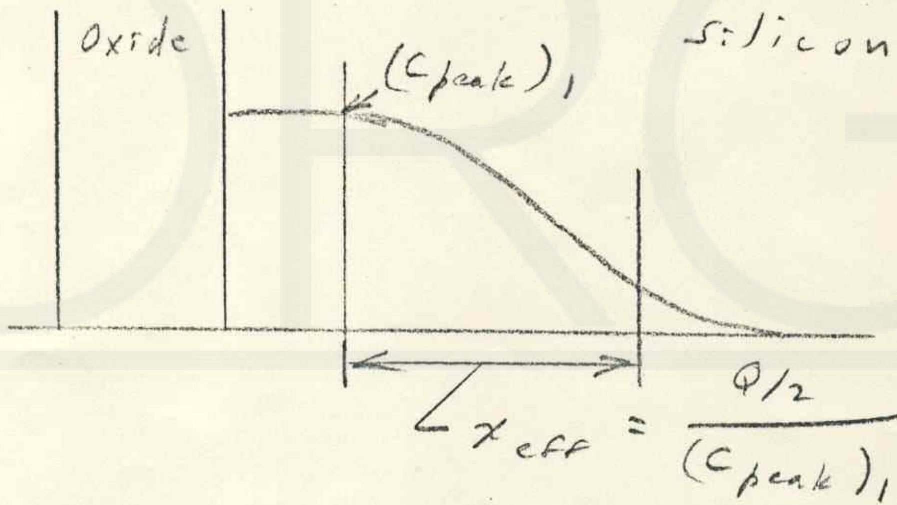

Figure 2

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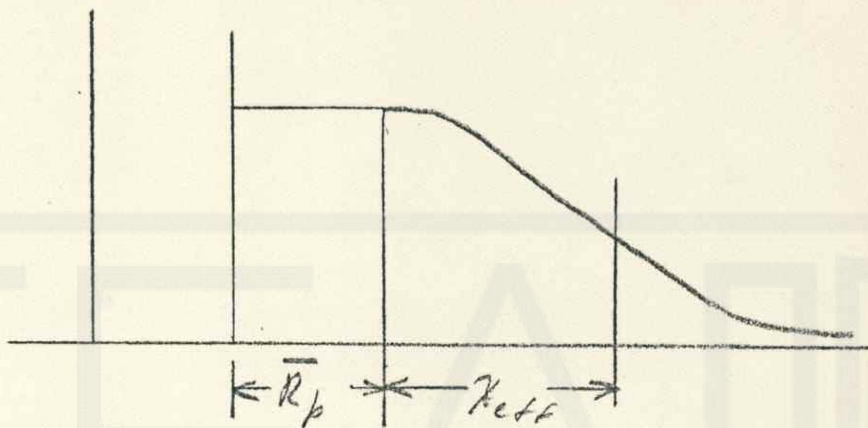

Figure 3

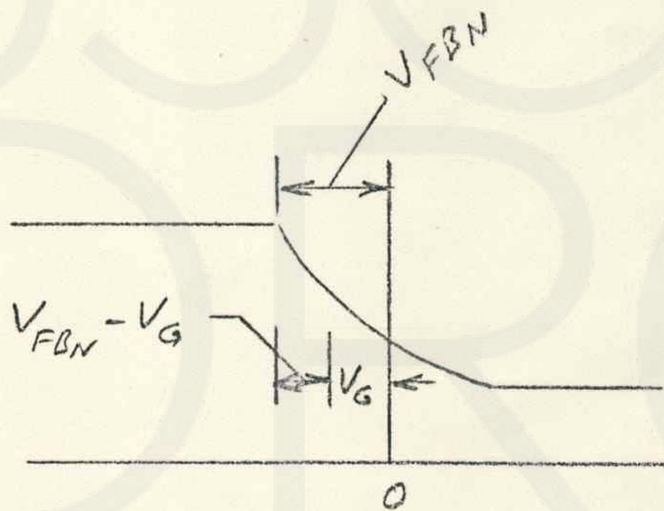

Figure 4

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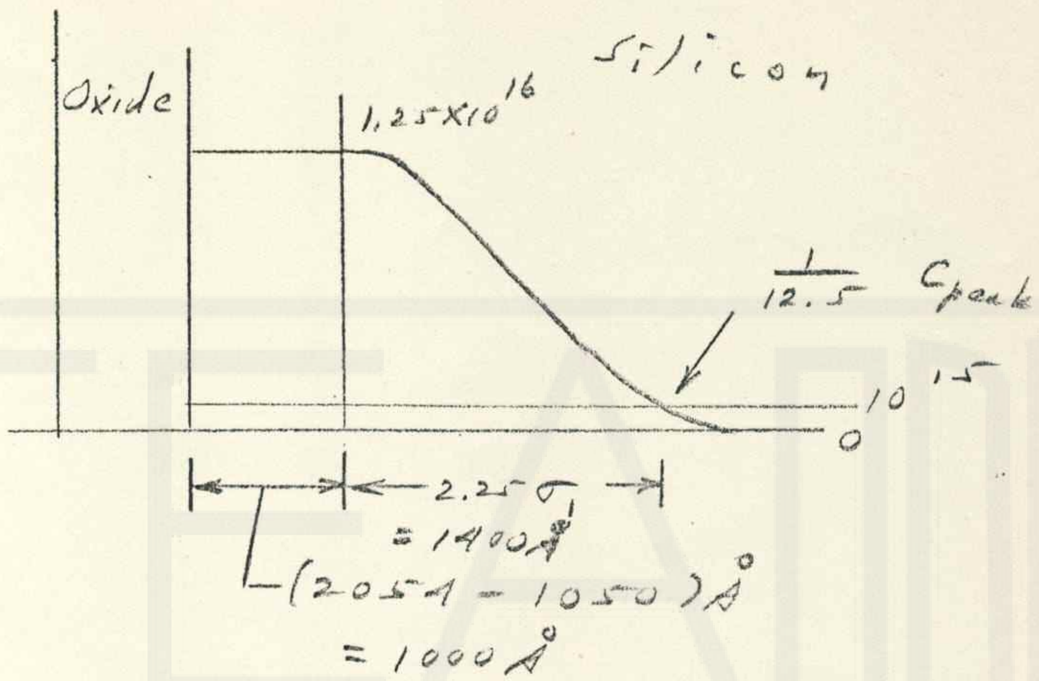

Figure 5

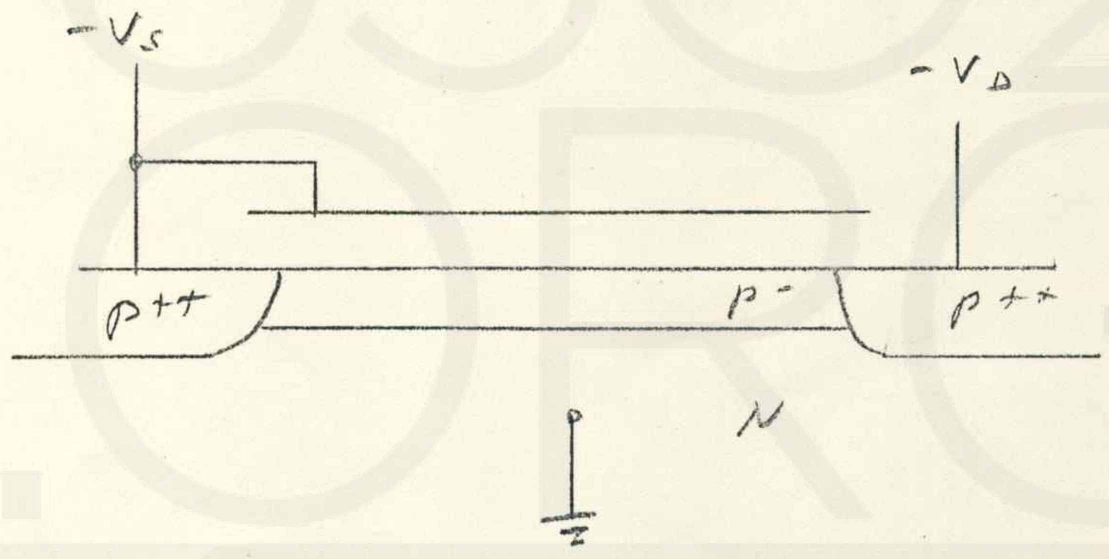

Figure 6

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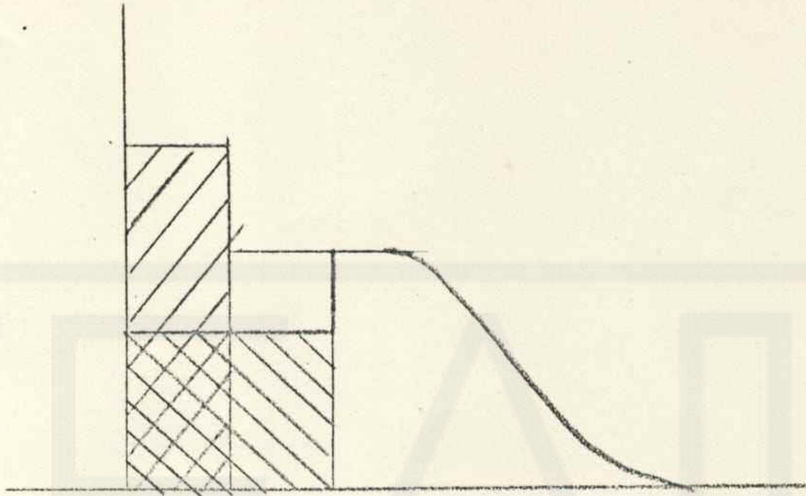

Figure 7

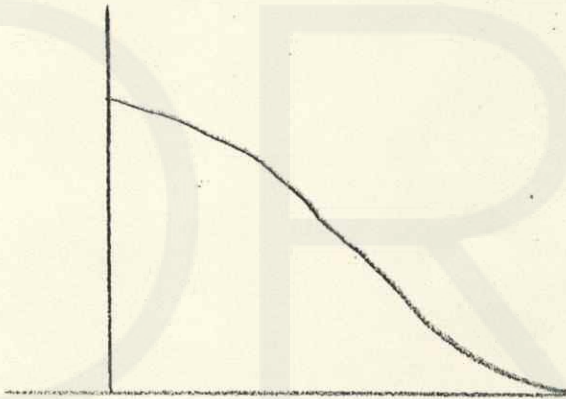

Figure 8

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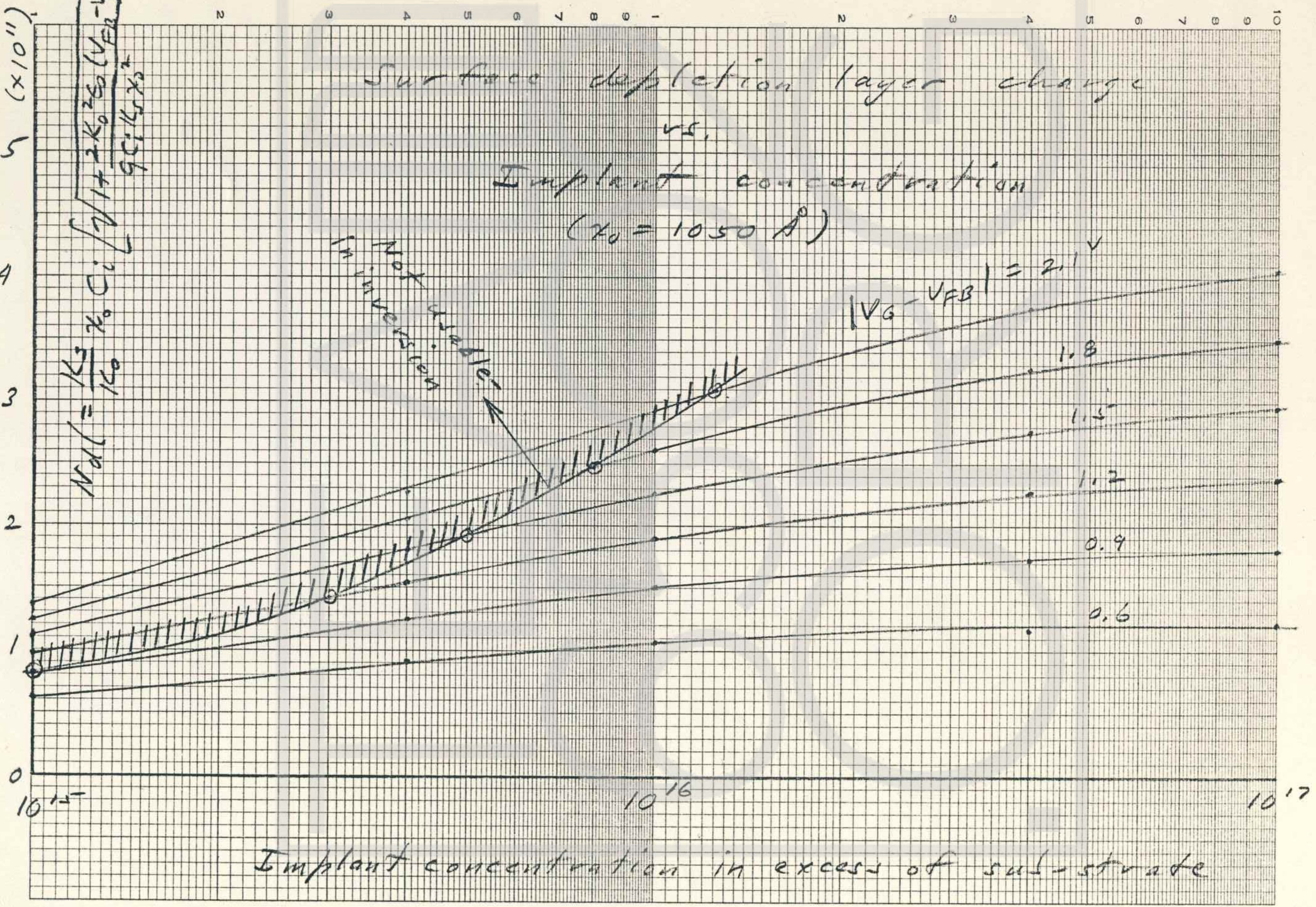
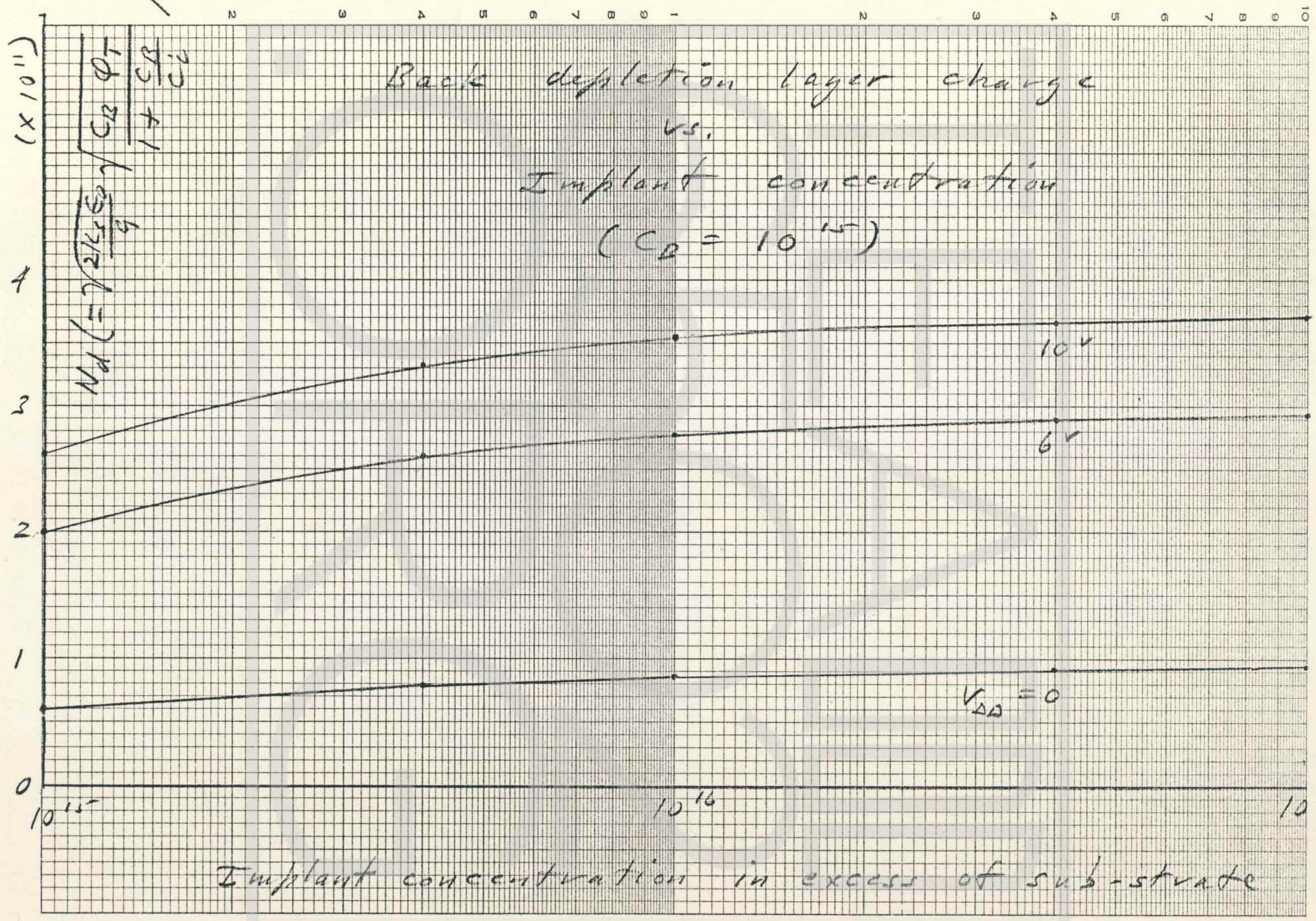


NO. 340R-L210 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
2 CYCLES X 10 DIVISIONS PER INCH
EUGENE DIETZGEN CO.
MADE IN U. S. A.
Surface depletion layer charge
vs.
Implant concentration
($x_0 = 1050$ Å)
$N_d \left(= \frac{K_S}{K_0} x_0 C_i \left[\sqrt{1 + \frac{2K_0^2 \epsilon_0 (V_{FB} - V_G)}{q C_i K_S x_0^2}} - 1 \right] \right)$
(×10^{11})
0
1
2
3
4
5
Not usable in inversion
$|V_G - V_{FB}| = 2.1$ V
1.8
1.5
1.2
0.9
0.6
10^{15}
10^{16}
10^{17}
Implant concentration in excess of sub-strate

NO. 340R-L210 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
2 CYCLES X 10 DIVISIONS PER INCH

EUGENE DIETZGEN CO.
MADE IN U. S. A.



Surface depletion layer thickness

vs.

Implant concentration

($x_0 = 1050$ Å)

$|V_G - V_{FB}| = 2.1$ V

1.8

1.5

1.2

0.9

0.6

Not usable — in inversion

$x_d \left(= \frac{V_d}{C_i} \right)$

10µ

1µ

0.1µ

0.01µ

10^{15} 10^{16} 10^{17}

Implant concentration in excess of sub-strate

EUGENE DIETZGEN CO.
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NO. 340R-L33 DIETZGEN GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

Back depletion layer thickness

vs.

Implant concentration

($C_B = 10^{15}$)

10μ

1μ

0.1μ

0.01μ

x_d ([illegible])

10v

6v

$V_{DD} = 0$

10^{15} 10^{16} 10^{17}

Implant concentration in excess of sub-strate

LOGARITHMIC
3 CYCLES X 3 CYCLES
MADE IN U. S. A.