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Depletion W/L = 4/.5 I = 50μA

Depletion-Mode IGFET Made by Deep Ion Implantation

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Abstract—p-channel depletion-mode IGFET's for use as depletion-load elements have been fabricated on ⟨100⟩ n-type 10-Ω·cm silicon using 120-keV boron ions implanted through the standard Bell Laboratories IGFET gate structure consisting of a double-layer dielectric of Al_2O_3 and SiO_2. The ion-implantation method is essential to achieve tight control of the boron impurity concentration in the IGFET channel, and is compatible with the standard fabrication process. The present implantation technique results in a Gaussian impurity profile with more than 97 percent of the implanted boron in the silicon beneath the Si–SiO_2 surface.

Since the boron profile is deep in comparison with the extrinsic Debye length for the boron concentration, the electrical behavior of the depletion IGFET's is controlled by the implanted subsurface behavior. The IGFET's are majority carrier devices best characterized by both a flat-band voltage and a drain saturation voltage, rather than a threshold voltage. A physical model for the subsurface channel has been developed and from this model current–voltage equations for the devices are derived assuming: 1) the conventional gradual channel approximation; 2) a weighted average profile to replace the Gaussian ion-implant profile; 3) a bulk mobility in the subsurface channel and an accumulation surface mobility for field-induced holes; and 4) a depletion approximation for the subsurface channel.

The theoretical results are in excellent agreement with experimental measurements of devices fabricated with a wide range of doses ($1–12\times10^{11}$ cm^{-2}) and a wide range of geometries. The experimental results indicate that no significant interface states were introduced during the implant–anneal process and that devices can be fabricated with predictable characteristics.

I. Introduction

When depletion-mode insulated-gate field-effect transistors (IGFET's) are used as circuit load elements in conjunction with enhancement IGFET's, the power-delay product can be increased by a factor of 3 or more over conventional all-enhancement circuits [1]. This improvement is due to the load line characteristics of depletion-load IGFET's with gate and source connected in common.

Several methods can be used to fabricate both enhancement and depletion IGFET's on the same wafer. For example, the gate metallization and insulator structures can be modified to change the effective metal–silicon work function difference which directly changes the threshold voltage. Another method of fabrication is the selective placement of donor or acceptor impurities into the IGFET channels. This can be done either by a doped-oxide diffusion or by ion implantation.

Ion implantation was chosen because exact control of the number of boron ions in the silicon is essential for reproducible device characteristics and because the boron concentration per unit volume ($\sim3\times10^{16}$/cm^3) is low, and therefore difficult to control by thermal diffusion. Ion implantation is also readily compatible with the standard IGFET process.

Ions implanted into silicon have a nearly Gaussian distribution profile provided that they are implanted at a small angle from the major crystallographic axes to avoid channeling. Implanting boron through an oxide such that only the leading edge of the Gaussian profile is in the silicon results in a device whose characteristics are similar to those of an unimplanted enhancement device, but which has a threshold voltage shifted by an amount proportional to the active implanted impurities in the silicon [2]. Although such a device may be modeled by simple device equations, this method results in the majority of the implanted impurities being left in the oxide, and reproducible device characteristics will be difficult to achieve. An alternate method is to use an ion energy sufficient to place the implant profile well beneath the silicon surface [3]. This will result in more reproducible p-channel depletion IGFET's because the implanted impurities in the silicon will be less sensitive to variations in process parameters such as oxide thickness, ion energy, and background impurity concentration. However, it will be shown that the device properties resulting from the deep implant require the development of a physical model for the subsurface channel. The resulting device is best characterized by

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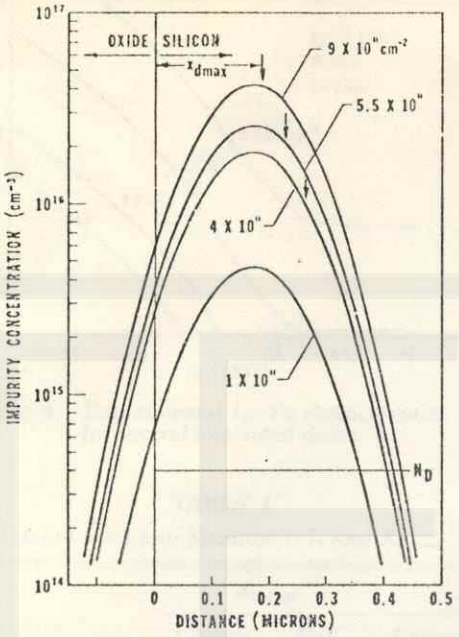

Fig. 2. Calculated profiles of the implanted boron (120 keV).

profile $\tilde{N}(x)$ is replaced by an average uniform profile $\overline{N}_A$, which is given by

$$\overline{N}_A = \int_0^{X_{d\,\max}} \tilde{N}(x)\,dx/X_{d\,\max}. \qquad (4)$$

Both $X_{d\,\max}$ and $\overline{N}_A$ can be iteratively calculated from (2)–(4) with N_A replaced by $\overline{N}_A$. The resulting $X_{d\,\max}$ values are indicated by arrows in Fig. 2.

For a low dose such as 1×10^{11} cm^{-2}, a surface field of about 1.5×10^{4} V·cm^{-1} can totally deplete the implanted region. However, for higher doses, larger than about 4×10^{11} cm^{-2}, the surface field can deplete holes from only a portion of the implanted region up to the maximum width indicated. Further increase of the surface field results in an inversion layer of electrons at the oxide–silicon interface which shields the subsurface channel from the surface field.

The influence of the surface field on the current behavior of a device with this subsurface channel can be easily understood by comparing the drain current I_D with the corresponding gate capacitance C_G. In Fig. 3, the measured C_G and I_D are plotted as a function of the gate voltage V_G for an ion-implanted device with a dose of 9×10^{11} cm^{-2}.

The C_G–V_G curve shown is a typical low-frequency curve that was obtained at the relatively high frequency of 100 kHz because electrons are supplied by an n-type ($\sim10^{17}$ cm^{-3}) diffusion normally used to increase the field oxide threshold voltage. This low-frequency behavior at 100 kHz is desired because the curve shows exactly the onset of strong inversion. Furthermore, the shape and width of the curve indicates whether significant interface states have been introduced by the implantation–anneal process. The capacitance at large negative voltages is solely that of the oxide due to the strong accumulation of holes at the oxide–silicon interface. The corresponding I_D in this region is thus large due to the presence of these accumulated holes. As the voltage increases positively, the density of the accumulated holes decreases, resulting in a decrease of C_G and a corresponding decrease in drain current. At a gate voltage of ~-0.8 V, labeled V_{FB} in Fig. 3, there are essentially no accumulated holes at the oxide–silicon surface and the current in the channel is due to the holes from the implanted acceptors. As V_G becomes more positive than V_{FB}, holes are depleted from the subsurface channel, which results in an increase in the surface depletion region and causes a further decrease in both C_G and I_D. This continues until V_G reaches a value, labeled $\phi_s=2\phi_F$ in Fig. 3, which is the beginning of strong inversion. For larger voltages, the increase of inversion electrons results in the observed rapid rise of C_G, which is predicted by the low-frequency MOS capacitance theory of a p-type surface. Since electrons in the inverted surface layer terminate the field lines from additional gate charge, little increase occurs in the depletion-layer width and consequently the current, which is due to holes, remains essentially constant.

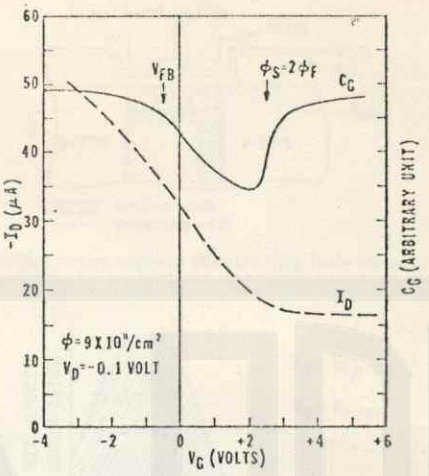

Fig. 3. Experimental C_G and I_D as a function of V_G.

The approximate value of the flat-band voltage, labeled V_{FB} in Fig. 3, also indicates that no significant increase in fixed charge was introduced by the implantation–anneal fabrication process. The observed $V_{FB}(\sim-0.8$ V) is within two-tenths of a volt of that expected from a theoretical calculation based on the average impurity doping value $\overline{N}_A(\sim2\times10^{16}/\text{cm}^{-3})$ for the implanted profile and the metal–semiconductor work function for that doping level. In addition, the width of the capacitance curve together with the voltage value for the onset of strong inversion indicates that no appreciable increase of the fast state density in the midgap region of the silicon bandgap has occurred.

A family of I_D–V_G curves is shown in Fig. 4 for several typical doses. As pointed out in the earlier discussion of the ion profile, the drain current for a dose of 10^{11} cm^{-2} can be decreased to zero by the gate field, whereas the current for a dose of 4×10^{11}/cm^{-2} ceases to be modulated at a voltage of approximately +2.3 V.