Walter D. Eisenhower, Jr.
1021 Sanderling Circle
Audubon, PA 19407
215-666-0343

SUMMARY: In the forefront of semiconductor technology since 1955 - managerial since 1962 - MOS since 1965. Set-up several facilities from scratch - several patents (including one of 3 basic NMOS processes), speeches, publications, etc. Equally at home with theory or hardware. Developed production processes for 6502 and Z-80A NMOS microprocessors and 1802 CMOS microprocessor. Seek opportunity to utilize unique breadth of experience in technically challenging pursuits - particularly partial to start-ups.

Areas of Technical Strength:

....MOS Processing - In 1965 developed the MTOS process which has become the industry standard. In 1968 developed the basic planox process. Metal and Silicon Gate PMOS, NMOS, CMOS and EPROM's.
....Planar Processing - Photolith (Positive Resist since 1965 - Perkin Elmer since 1974), Diffusion, Oxidation, Pyrolytic Coating (since 1958), Metallization and all phases of assembly processing.
....Thin and Thick Film Hybrids - Tantalum-Nitride Thin Films and Cermet Thick films including High Frequency Capacitors.
....Passivation Techniques - Vapor Deposition at Atmospheric Pressure or Reduced Pressure, Sedimentation, High Vacuum Evaporation and Sputtering;
....Pyrolytic PSG overlay - industry first - introduced at G.I. (1967). Presently doing plasma enhanced SINCAP for overlay and Plasma Enhanced BPSG for intermediate field (Deposited plasma nitride in 1965)
....Material Processing - Refining; Crystal Growth - Czchrolski, Rate Grown, Float Zone, Zone Leveling; Epitaxy; Polishing; Gas Etching.
....Reliability Evaluation - Step Stress, etc. In charge of Minuteman Qualification, Production, TEsting for GE DBT; Introduced Vycor Getter and BaO-SrO getters.
....Device Design - Planar Diodes, Transistors, High Frequency Transistors, Silicon Controlled Switch, MOSFETS: Flip-Chips; Beam-Leads.
....Proposal Writing - Cost Estimating, Forecasts, PERT, Detailed Manufacturing Procedures, Cost Reduction, Learning Curves (Cost Improvement Curves).

EMPLOYMENT HISTORY: Oct. 1979 to present - MOS Technology, Inc.
Manager, Advanced Process Development

Developed production techniques for NMOS Product line making nearly 10,000 starts per week of 4" using 5 micron rules. Presently phasing-in 4 micron process and developing 3.5 process - utilizing latest technology - plasma etching, and deposition, cassette-to-cassette sputtering, etc. Consultant to sister division bringing 5" line on stream.

Apr. 1977 to Oct. 1979 - Solid State Scientific
Manager, Advanced Process Development

Hired to develop C^2L process for 1802 CMOS Microprocessor. Developed Silicon Gate CMOS process for 5101 RAM. Developed High-Rel PSAG for Vinson. Introduced LPCVD Poly, Nitride, LTO Oxide.

March 1969 to April 1977 - MOS Technology, Inc.
Manager, Advanced Process Development

Developed production process for 6502 family of microprocessors (Patent issued on process). Several other patents issued and pending. One of five people who founded the company. Designed facility, hired staff, developed all processes (PMOS - video games, calculators, RAMS and NMOS - microprocessors, ROMS, RAMS etc.)

Sept. 1965 to Feb. 1969 - General Instrument Corporation
Microelectronics Division
Manager, Advanced Process Development

Developed MTOS process which has become the industry standard utilizing low temperature oxidation to create thick fields without excessive diffusion. Also used phosphorus passivation and protective overlay dielectric. Developed basic Planox process for low threshold devices in 1968. Improved performance, reliability, and cost. Major contributions to yield improvement. Investigated new dielectrics and passivation techniques (Nitride and Alumina).

Jan. 1965 - Sept. 1965 - ITT Federal Laboratories
Microelectronics Department
Manager - Thin Film Department

Fabrication of thin film hybrid circuits for digital and linear applications. Introduced thick film techniques to supplement thin films for low cost but achieved performance gains as well by successfully developing capacitors with usable Q at 100 MHz. Left because scope of programs and funding had been misrepresented.

Feb. 1962 - Dec. 1965 - Burroughs Corporation
Electronic Components Division
Manager, Semiconductor Development Dept.

Established semiconductor facility from scratch. Recruited staff, installed facilities, developed processes for proprietary line of multiple element packages of planar diodes, transistors and silicon controlled switches for encoding, decoding Nixie Drivers with/without memory, counters, etc. Independently conceived flip chip hybrid assembly technique which IBM was also developing. IBM awarded basic patents on SLT; however, several specific patents awarded. Completed mechanization of packaging and assembly.

Sept. 1955 - Jan. 1962 - Western Electric
Laureldale, Pennsylvania
Senior Engineer

55 - 57: Crystal growth and related; developed fool-proof zone leveler for dislocation-free germanium.
58 - 60: Product Engineer Germanium DBT for Nike ZEUS and Minuteman. Improved reliability from 2% AQL to 0.5% AQL without getters, then introduced VYCOR and later Barium Oxide Getter.
60 - 61: Product Engineer - Silicon Planar Transistor (2N914) Diffusion consultant for all product lines.

June 1951 - Sept. 1955 - Empire Steel Castings
Assistant Metallurgist

Responsible for chemical, metallurgical, radiographic laboratories, melting department, welding and stainless heat treating. Developed melting techniques for 304L and 316L stainless steel (0.03C max.).

EDUCATION: University of Pennsylvania, 1945-47, Chem. Eng.
Albright College, B.S. 1951
Penn State University Graduate - One year, Solid State Physics
Western Electric Graduate Center - Courses in Semiconductor Technology, Engineering Materials, Statistics, SQC.
Motorola - Integrated Circuits Design Course

PERSONAL: Born January 14, 1928 - Reading, Pennsylvania.
Married, five children, own home. USN Honorable Discharge.
Secret Clearance. 5' 7½" - 160 lbs.

OTHER: Several patents issued and others pending.
Published "The Evolution of the Horizontal Crystal Grower," The Western Electric Engineer
Technical Speeches - Cornell, Virginia Polytech plus IEEE, ASME Local Chapters, etc.
Taught a course on "Semiconductor Fundamentals" for new engineers at Western Electric and Bell Telephone Laboratories
Cost Reduction Awards at Western Electric Company
Presented "Material Aspects of MOS Processing" at MRC Conference (1974)

WALTER D. EISENHOWER, JR.

EMPLOYMENT HISTORY

APPROXIMATE DATE(S)	JOB
1939 11 yrs old	MAGAZINES (COLLIERS,LHJ,SEP)
1940	PAPERS @ FARMERS MARKET
	REGULAR MORNING PAPER ROUTE
1941	L.D.MOYER'S GROCERY(TO 1944)
1942	A.S.BECK SHOES
1943	MOHN'S HAT FACTORY
	PA FREIGHT STATION
1944	AMERICAN SAFETY TABLE
	L.D.MOYER
1945	OUTDOOR ADVERTISING
	U.S, NAVY(ACTIVE DUTY 45TO47) Student @ Penn
	(INACTIVE 47 TO 53)
1947	LABORER
	HOD CARRIER
	WASHING CARS
1948 20 yrs old married in June	CHEMIST PLASTICS(PVC)
	CASTINGS INSPECTOR
	STUDENT (ALBRIGHT)TO '51
	WELDER (TO '50)
	LABORER(SPRING BREAK)
1951	EMPIRE STEEL CASTINGS
	GRINDERWELDER CHEMIST
1952	ASSISTANT METALLURGIST
1953	TEACHER-RHS EVENING SCHOOL
1954	ENGINEER – WESTERN ELECTRIC
1962	MANAGER-SEMICONDUCTOR
	DEPARTMENT- BURROUGHS(NJ)

DATE(S)	JOB
1963	BURROUGHS(NJ)
1964	MANAGER – MICROELECTRONICS DEPT – ITT(NUTELY N.J.)
1965	MANAGER S.C.DEPT-G.I. (NY)
1969	MANAGER S.C. – MOS TECH (PA)
1976	MGR – COMMODORE INT'L(PA)
1984	MGR FRONTIER DIV (CA)
1985	MGR,FRONTIER DIV
1986	MGR FRONTIER/MOS DIV(CA/PA)
1987	MGR-COMMODORE INT'L TO '92
1992	RETIRED
1994	EXEC VP AND CTO GMT(PA)
1998 to 1999 71	LEFT GMT, BECAME CONSULTANT
2000 72	CONSULT GMT,MNC,VISHAY,LSI
2001 73	CONSULTING SAME AS '00
2002	RETIRED AGAIN
2003	FAMILY AND CHURCH

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